PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application	:	David C. Davies et al.
Serial No.	:	
Filed	:	Herewith
For	:	Flexible Processing Hardware Architecture
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PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the initial review of this non-provisional divisional utility patent application entitled "Flexible Processing Hardware Architecture" by David C. Davies, Michael P. Greenberg, Michael J. Wilt, and John E. Agapakis, please amend the above-identified Patent Application as follows:

In the specification:

Page 1, after the title, please insert the following

paragraph: --This application is a divisional of U.S. Patent Application No. 09/030,411, filed February 25, 1998.--

In the claims:

Please cancel claims 1 through 12 and 14 through 22. This divisional application will prosecute claim 13.

Please add the following new claims 23-40:

23. A vision processing system comprising:

a host processing system including a host central processing unit (CPU) and a host peripheral component interconnect (PCI) bus coupled to said host CPU; and

at least one vision processing subsystem implemented as a PCI add-in extension board coupled to said host processing system, said at least one vision processing subsystem including a local PCI bus, a peripheral bus bridge coupling said local PCI bus to said host PCI bus, at least one PCI device coupled to said local PCI bus, and means for hiding said at least one PCI device from said host processing system.

24. The vision processing system of claim 23 wherein said at least one vision processing subsystem includes a plurality of vision processing subsystems implemented on a plurality of PCI add-in extension boards.

25. The vision processing system of claim 23 wherein said at least one vision processing subsystem includes a digitizer subsystem.

26. The vision processing system of claim 25 wherein said PCI device includes a camera interface in said digitizer subsystem.

27. The vision processing system of claim 23 wherein said at least one vision processing subsystem includes a vision processing accelerator subsystem.

28. The vision processing system of claim 27 wherein said PCI device includes a processing accelerator in said vision processing accelerator subsystem.

29. The vision processing system of claim 23 wherein said at least one vision processing subsystem includes an embedded CPU subsystem having an embedded CPU.

30. The vision processing system of claim 29 wherein said PCI device includes a display controller in said embedded CPU subsystem.

31. The vision processing system of claim 29 wherein said PCI device includes a host bus bridge coupled to said embedded CPU in said embedded CPU subsystem.

32. The vision processing system of claim 23 wherein said means for hiding said PCI device includes a connection of an identification selection (IDSEL) line of said PCI device to a PCI address line of said local PCI bus in a range of AD[31:16] and a means for temporarily disabling said IDSEL line.

33. The vision processing system of claim 23 wherein said means for hiding said PCI device includes means for controlling a reset release signal and identification selection (IDSEL) signal

to temporarily disable said PCI device from said local PCI bus.

34. The vision processing system of claim 23 wherein said means for hiding said PCI device includes a complex programmable logic device (CPLD) and a state machine for controlling a reset release and for controlling identification selection (IDSEL) connection sequencing to temporarily disable said PCI device from said local PCI bus.

35. The vision processing system of claim 29 further including a back-door signal between said peripheral bus bridge and said embedded CPU subsystem, for resetting said embedded CPU subsystem if said embedded CPU subsystem locks up.

36. A configurable vision processing system for connection to a personal computer (PC), said configurable vision processing system comprising:

a local peripheral component interconnect (PCI) bus;

a vision accelerator subsystem coupled to said local (PCI) bus, said vision accelerator subsystem including a processing accelerator and at least one image memory interfaced with said processing accelerator;

a digitizer subsystem coupled to said local (PCI) bus, said digitizer subsystem including a digitizer and at least one camera coupled to said digitizer; and

a vision central processing unit (CPU) subsystem coupled to said local (PCI) bus, said vision CPU subsystem including an embedded vision system CPU, a host bus bridge for interfacing said vision system CPU to said local (PCI) bus, system memory, at least one system peripheral, and a display controller for interfacing a local display to said local (PCI) bus.

37. The configurable vision processing system of claim 36 further including a peripheral bus bridge coupled to said local PCI bus, wherein said peripheral bus bridge is adapted to be coupled to a host PCI bus within said PC such that said configurable vision processing system is implemented as a PCI add-in extension board.

38. The configurable vision processing system of claim 37 wherein said display controller has an identification selection (IDSEL) line connected to a PCI address line of said local PCI bus in a range of AD[15:11] and wherein said host bus bridge has an

IDSEL line connected to a PCI address line of said host PCI bus in a range of AD[31:16].

39. The configurable vision processing system of claim 38 wherein said vision CPU subsystem includes means for controlling a reset release and an identification selection (IDSEL) connection sequencing of devices connected to said local PCI bus to temporarily disable said devices from said local PCI bus.

40. The configurable vision processing system of claim 37 further including a back-door signal between said peripheral bus bridge and said vision CPU subsystem, for resetting said vision CPU subsystem if said vision CPU subsystem locks up.

REMARKS

The examiner is invited to telephone the undersigned, applicant's attorney of record, to facilitate advancement of the present application.

Respectfully submitted,

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